

FIG.1

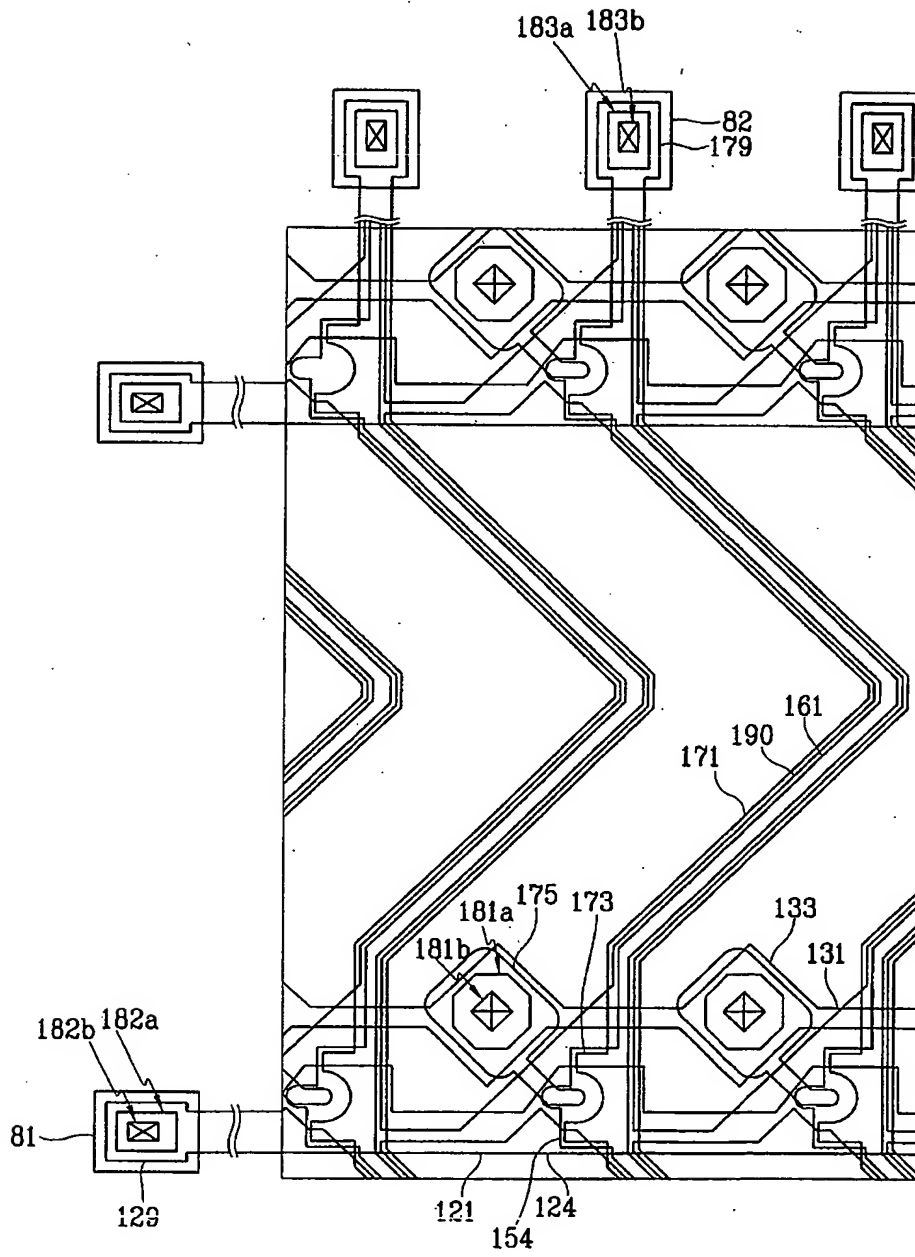


FIG.2

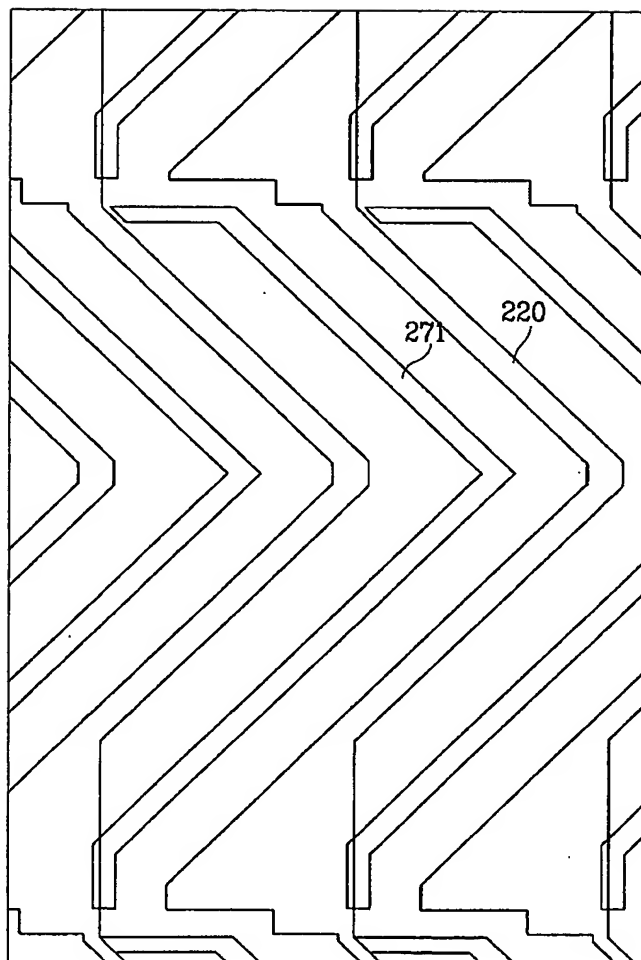


FIG.3

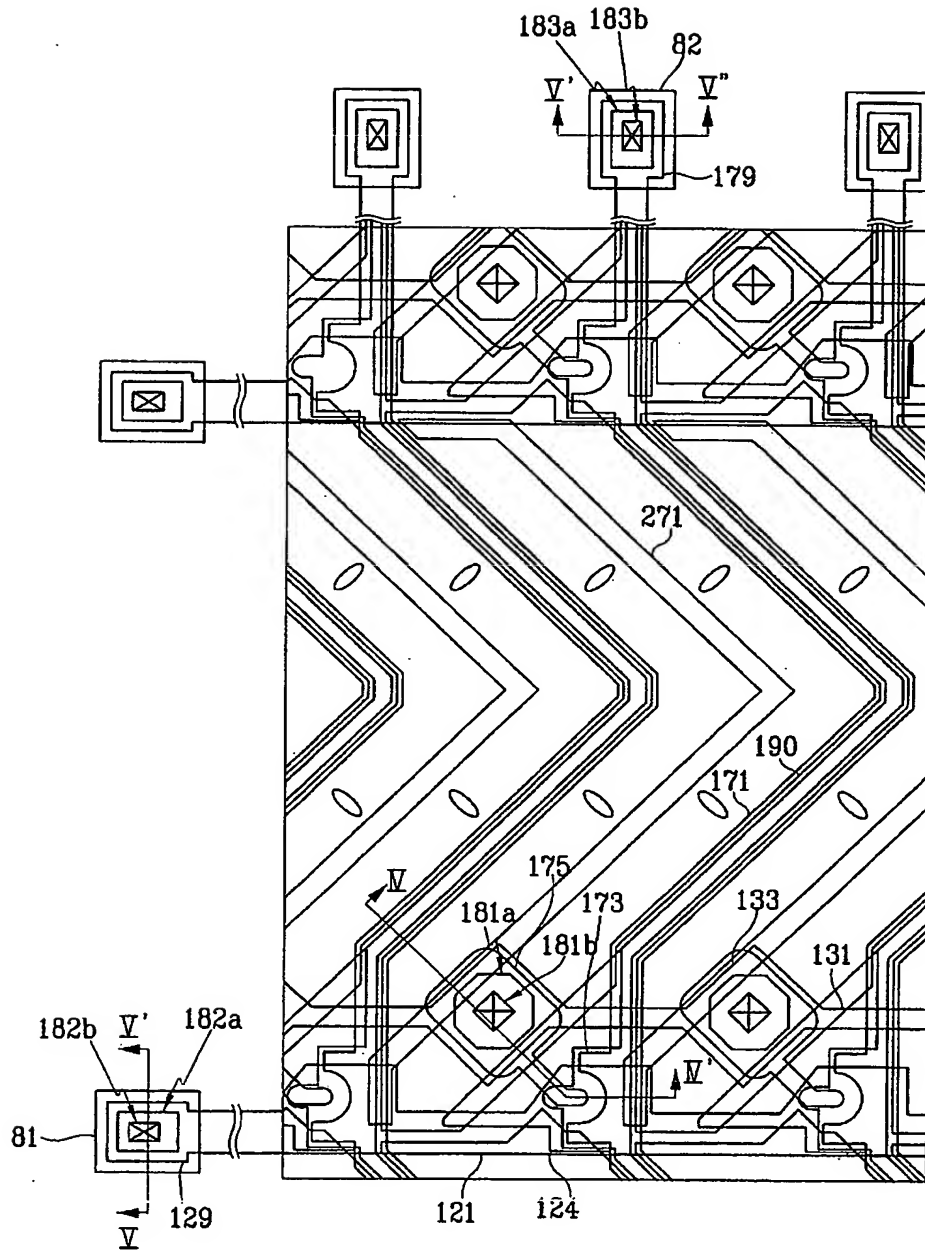


FIG.4

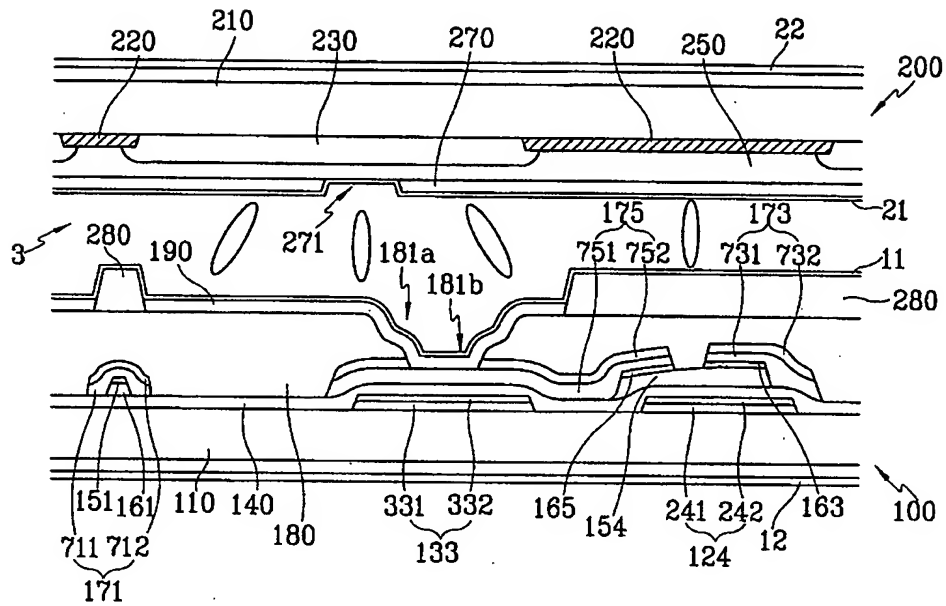


FIG.5

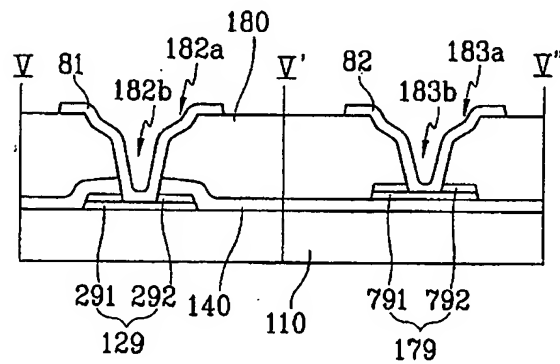


FIG.6A

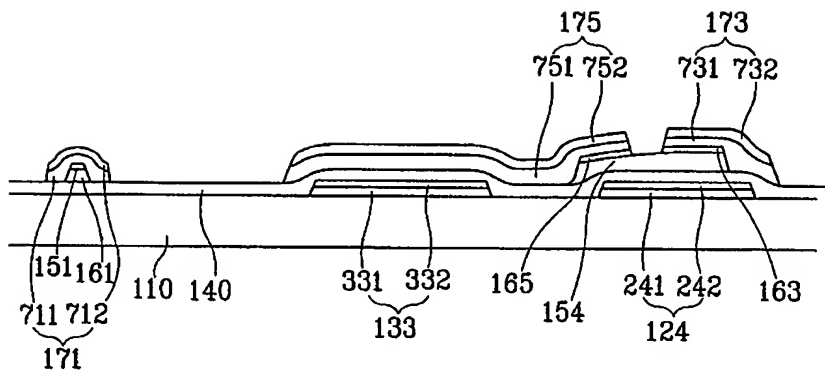


FIG.6B

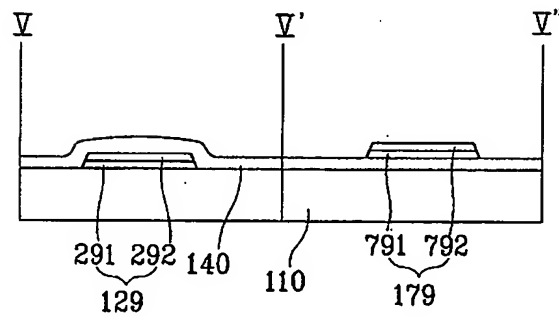


FIG.7A

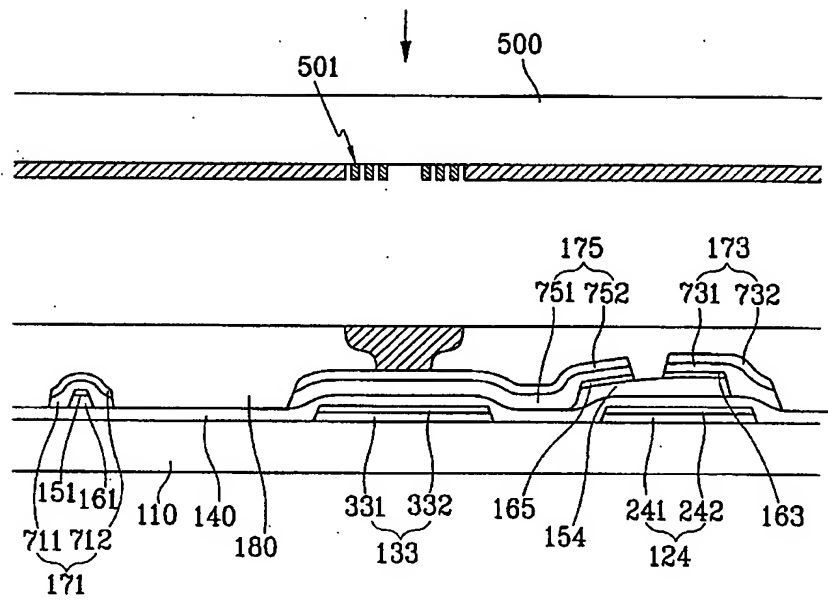


FIG.7B

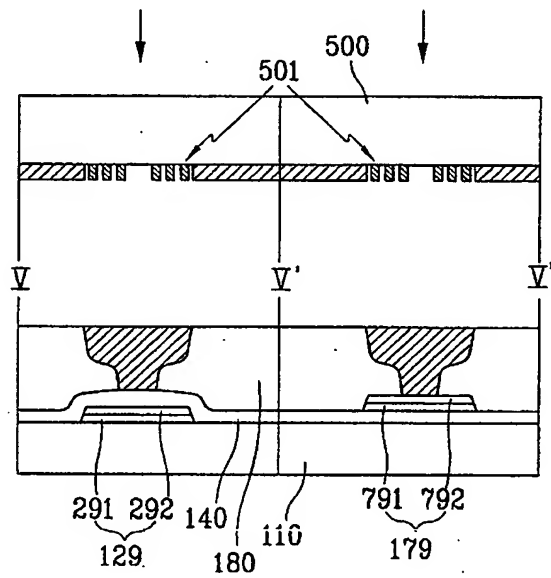


FIG.8A

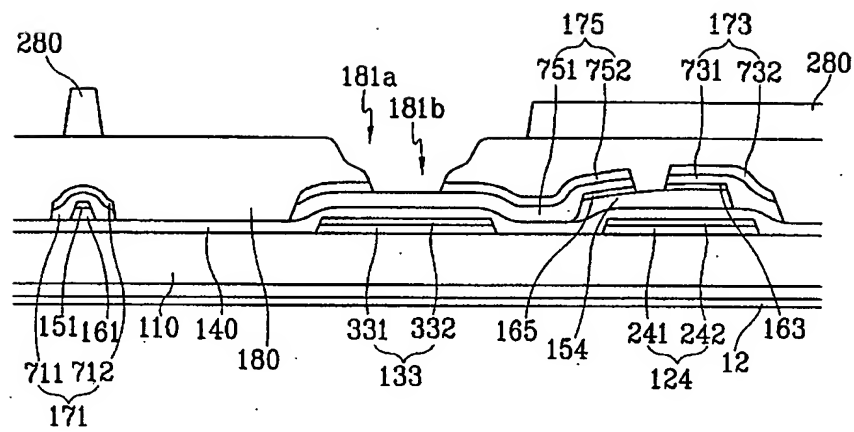


FIG.8B

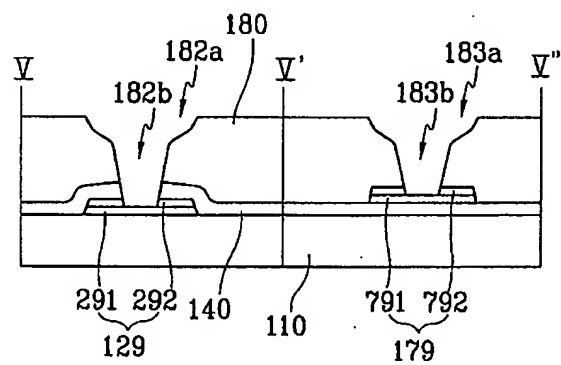
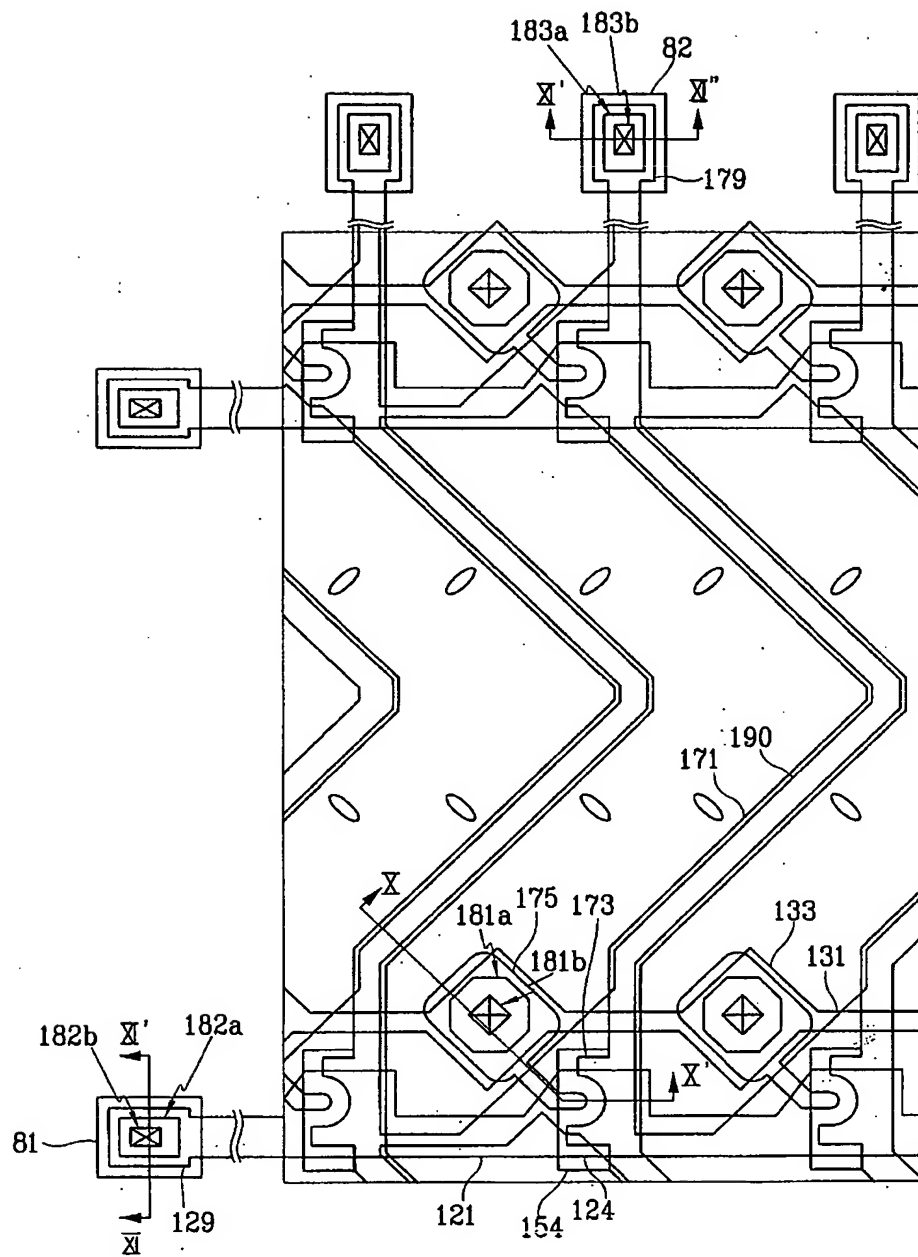


FIG.9





[illegible]

FIG.12A

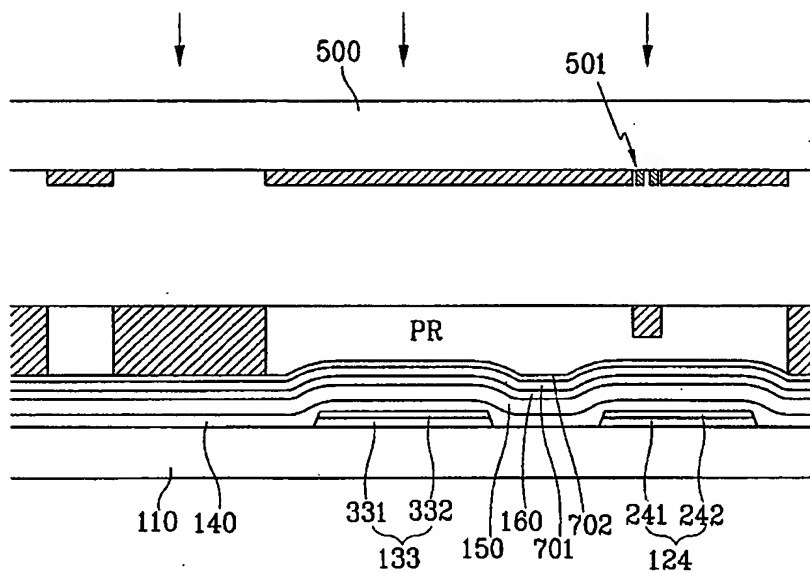


FIG.12B

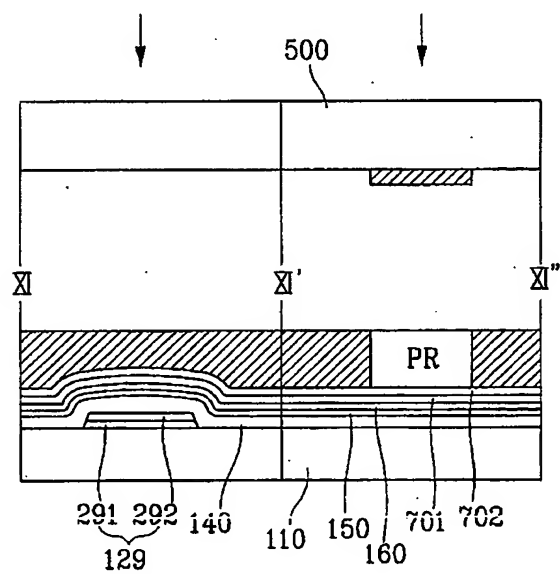


FIG.13A

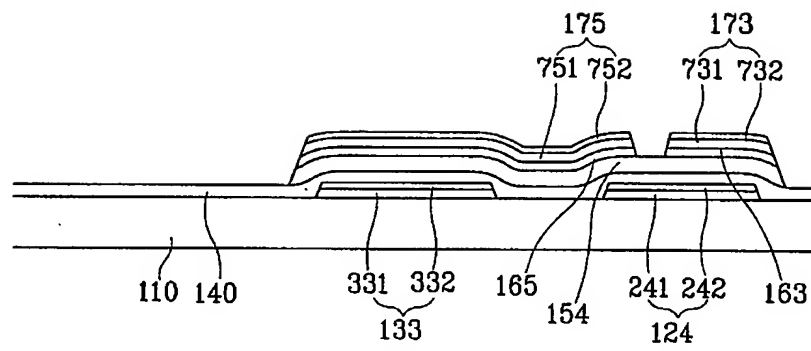


FIG.13B

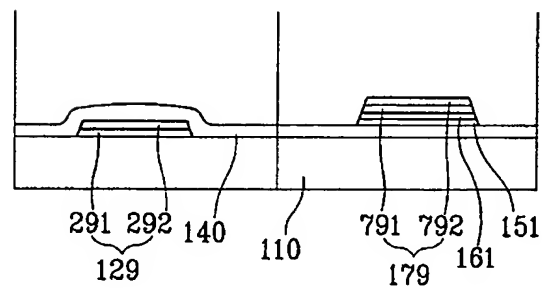


FIG.14A

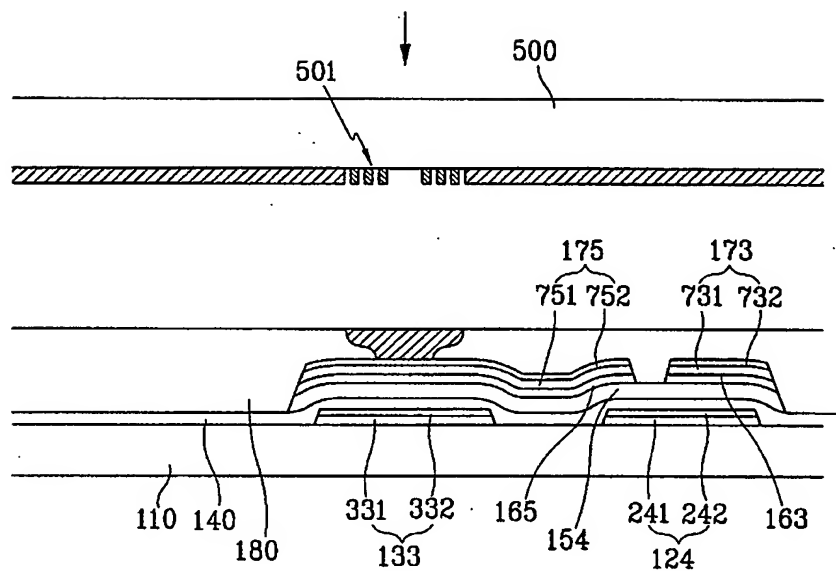


FIG.14B

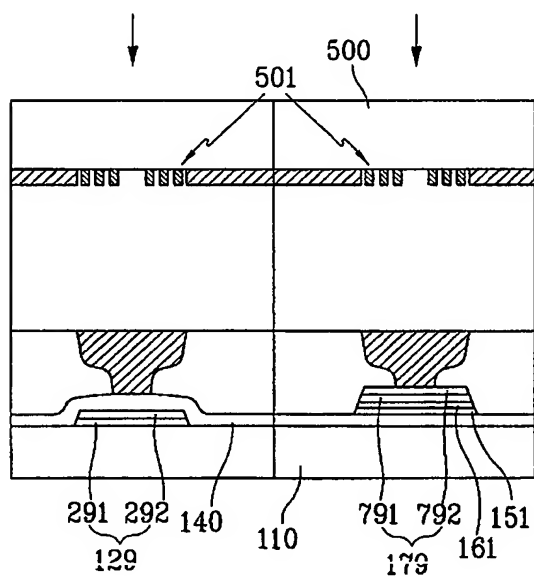


FIG.15A

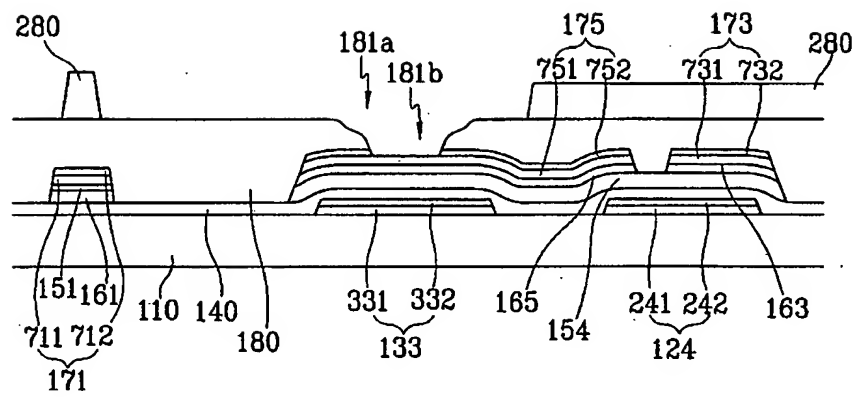


FIG.15B

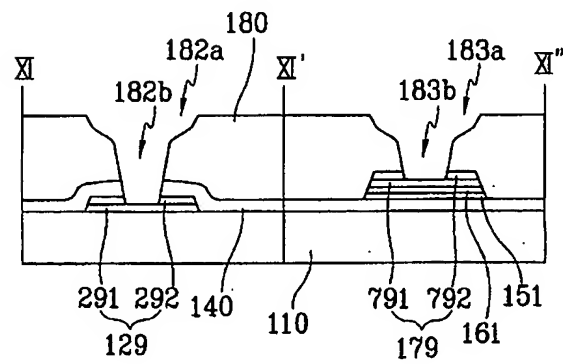
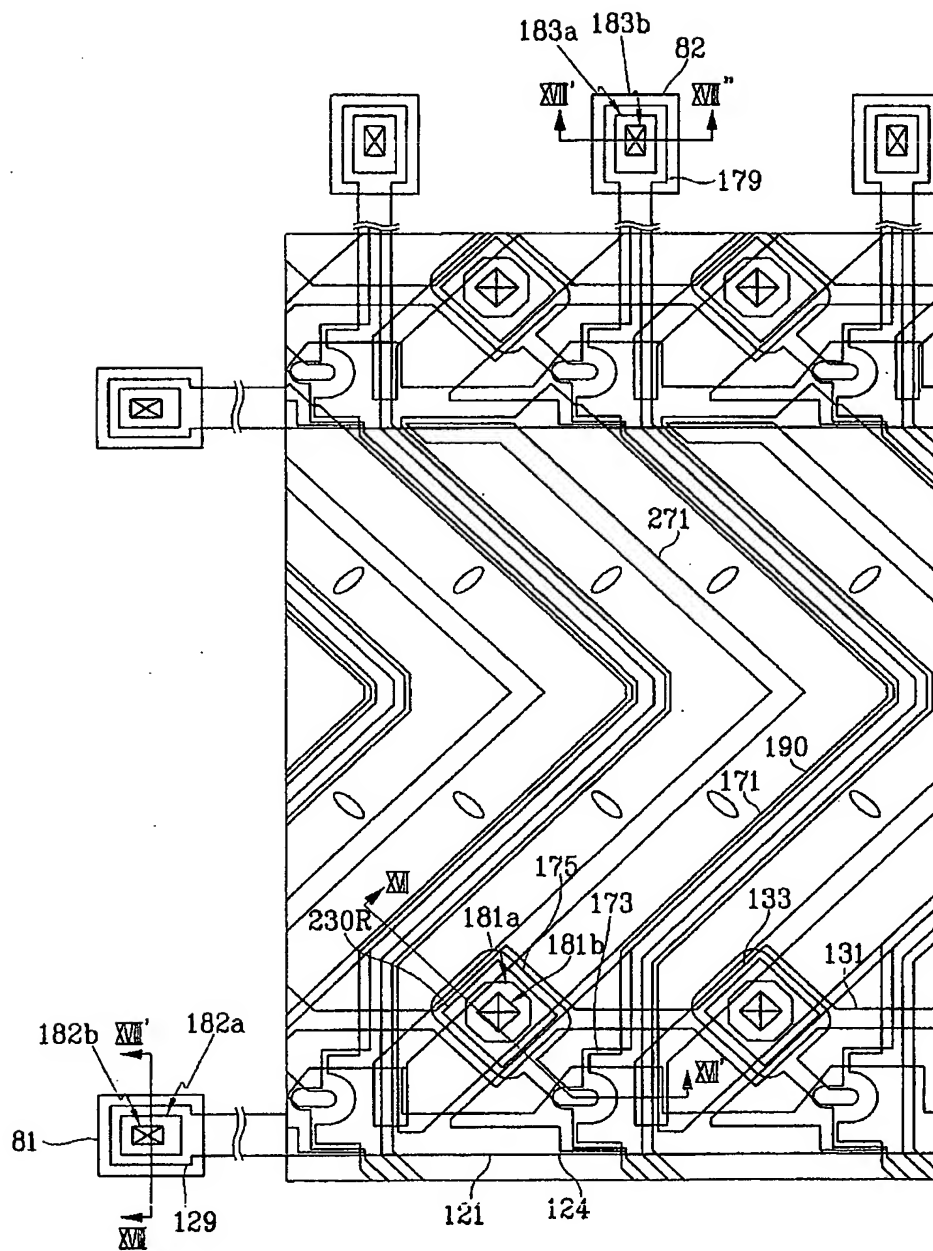


FIG.16



This cross-sectional view shows a semiconductor device with two gate structures. The substrate 110 is divided into two regions, 129 and 179, by a central layer 140. Region 129 contains a gate stack 81 with a gate dielectric 801 and a gate electrode 802. A gate trench 182 is formed in the gate stack 81, with its side walls labeled 182a and 182b. Region 179 contains a gate stack 82 with a gate dielectric 791 and a gate electrode 792. A gate trench 183 is formed in the gate stack 82, with its side walls labeled 183a and 183b. The device is bounded by cross-sections XX' and XX'.

FIG.19

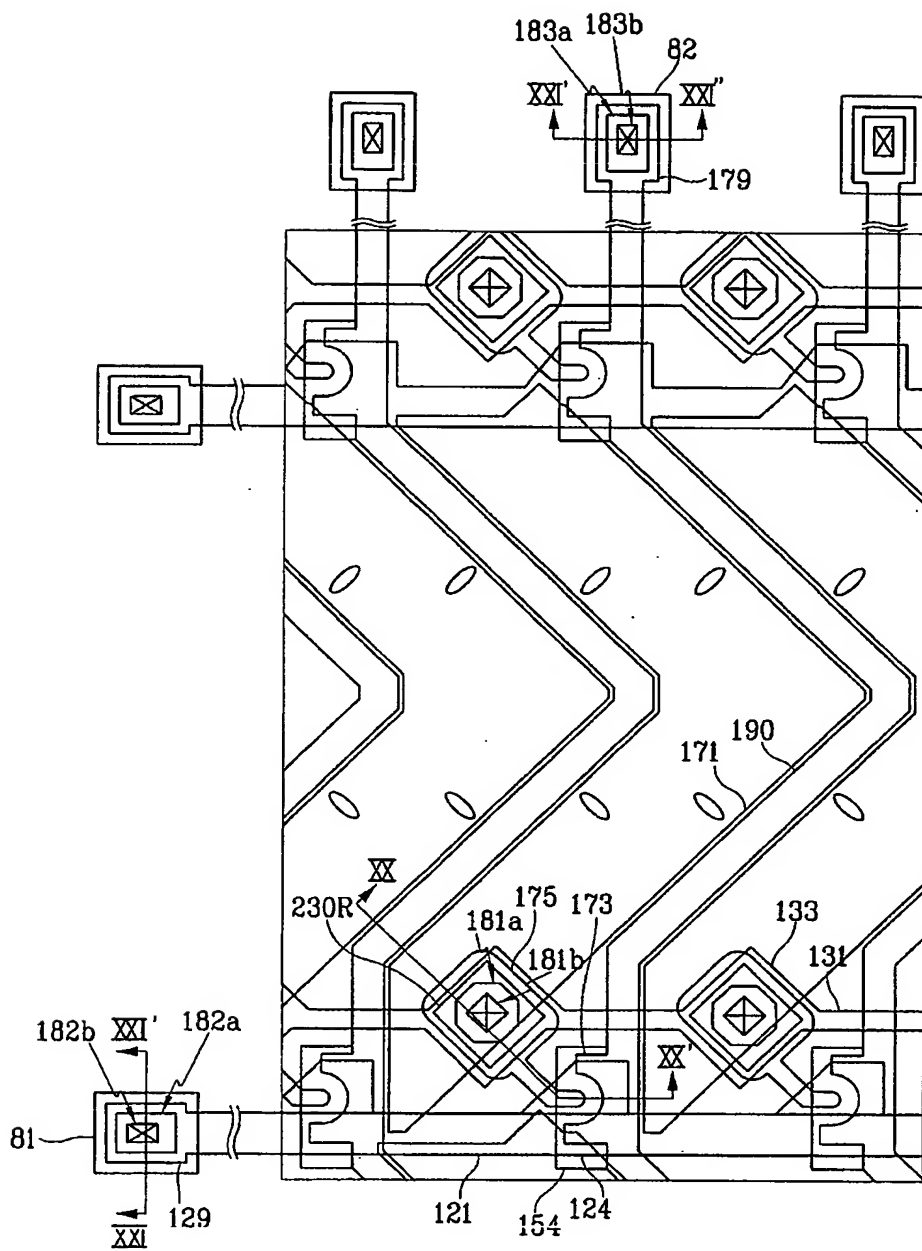




FIG.20

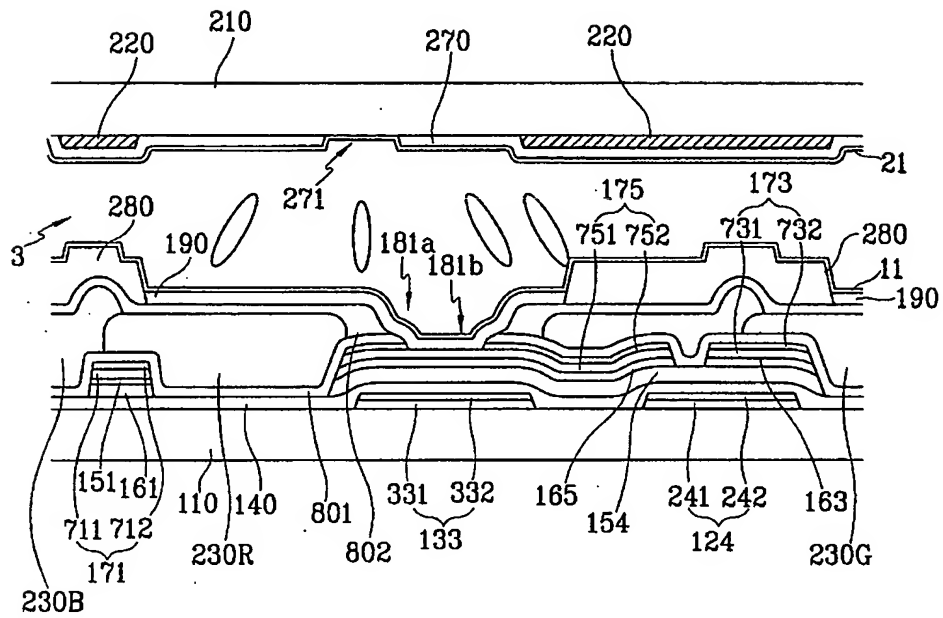


FIG.21

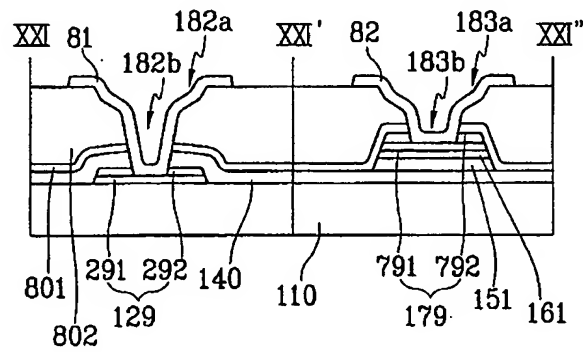


FIG.22

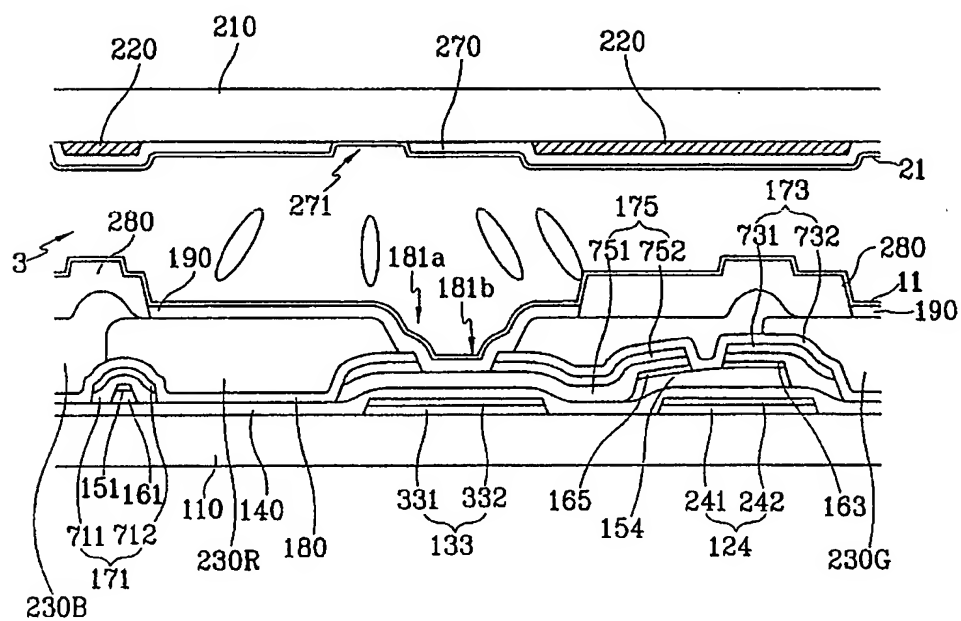
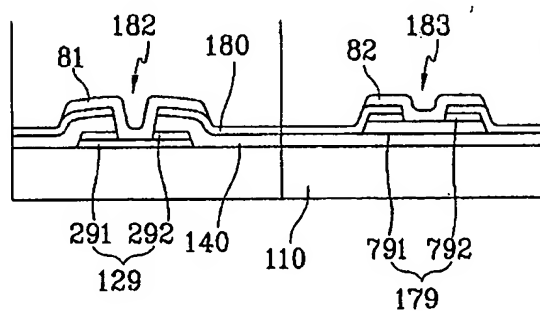


FIG.23



[illegible]

FIG.26

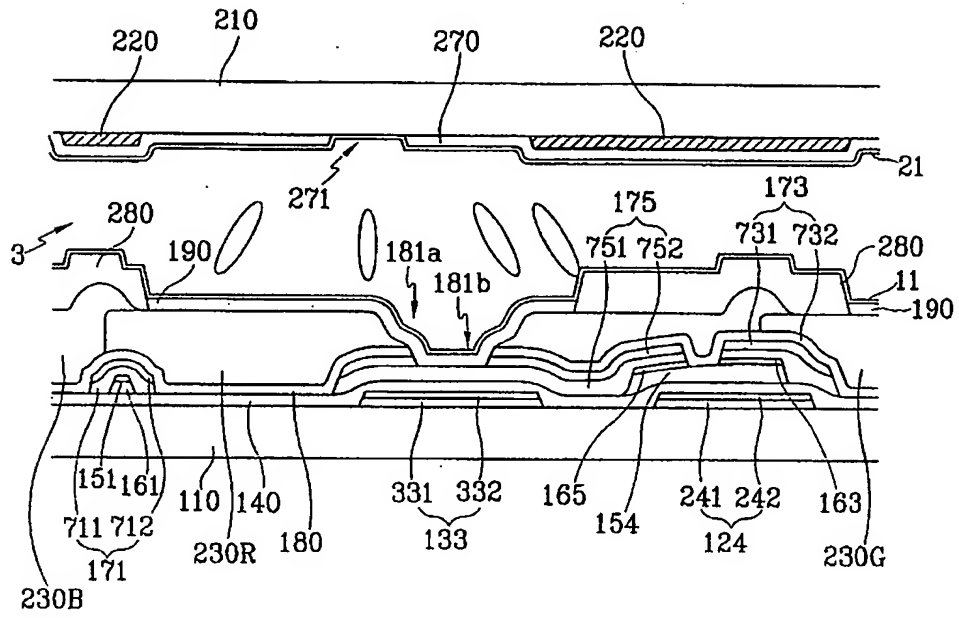


FIG.27

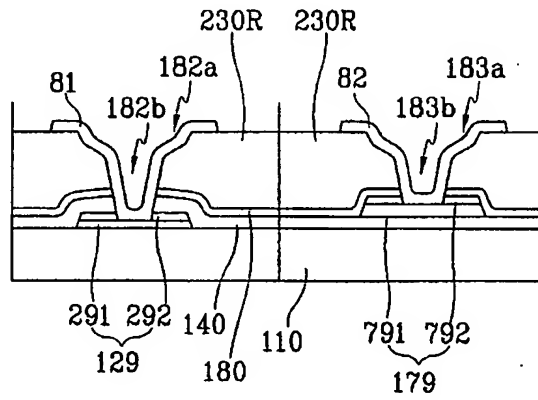


FIG.28

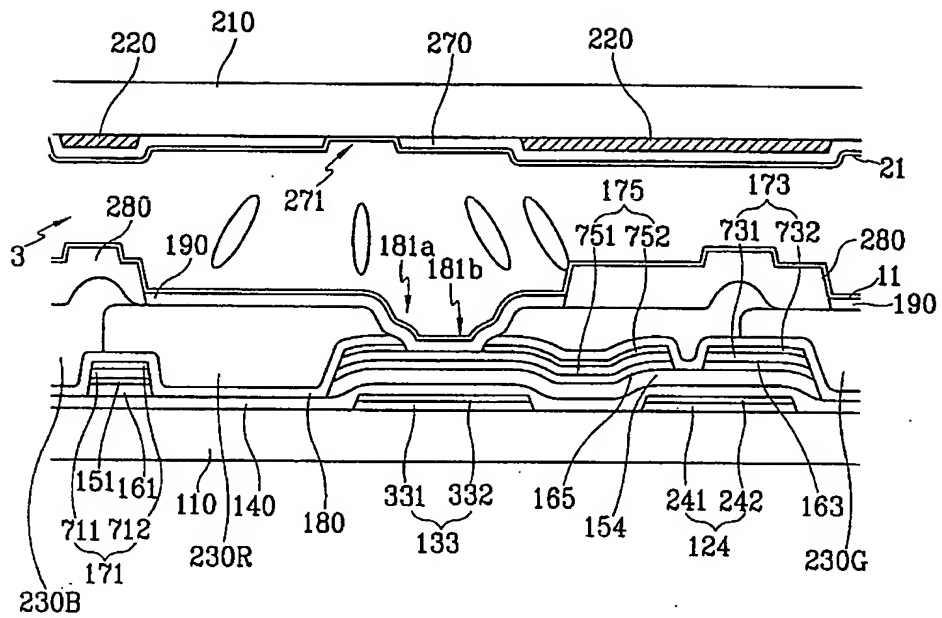


FIG.29

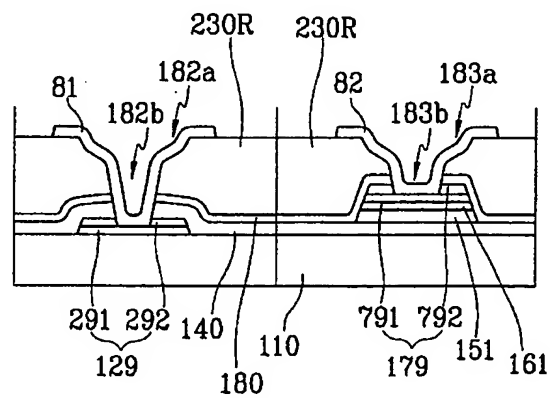


FIG.30

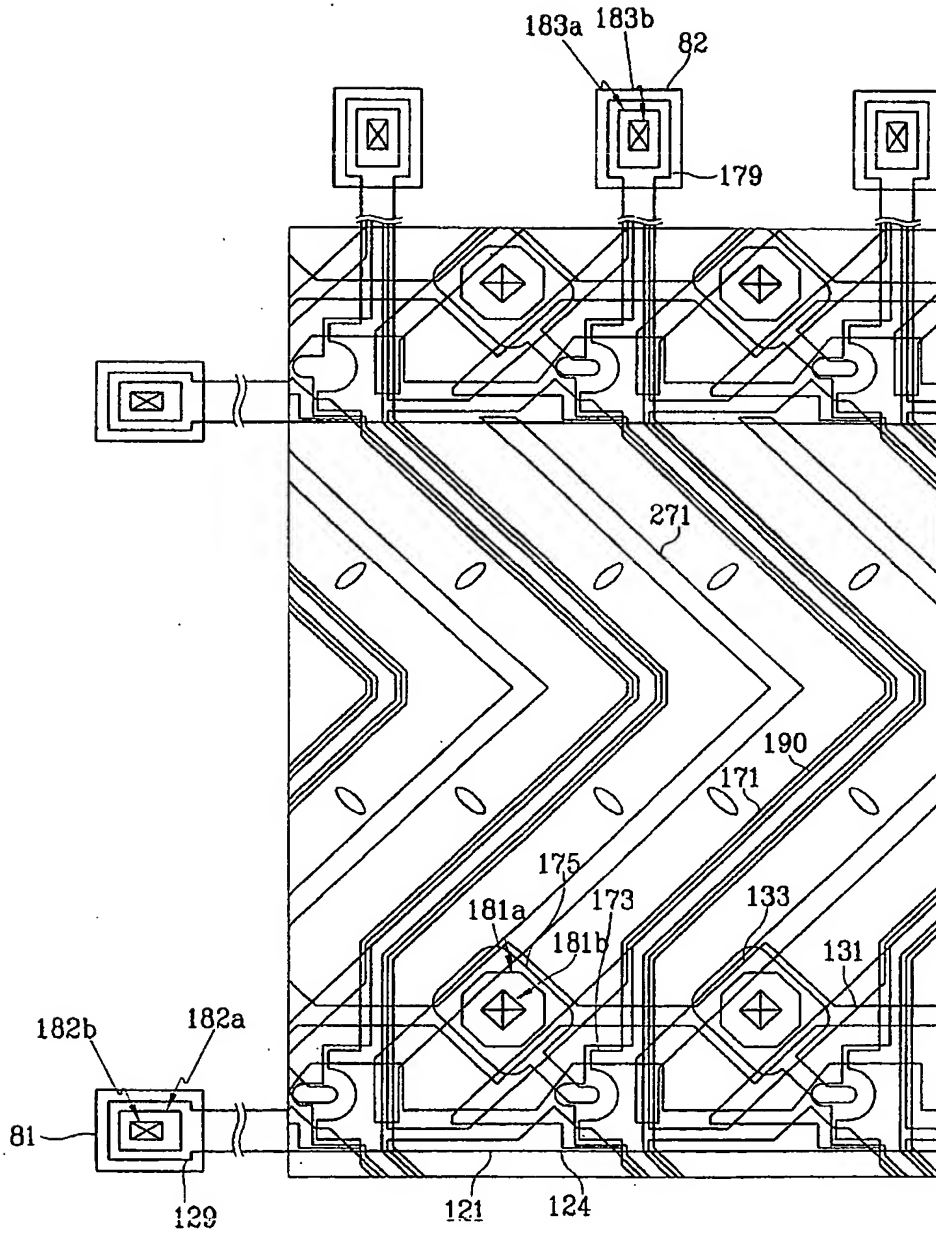


FIG.31

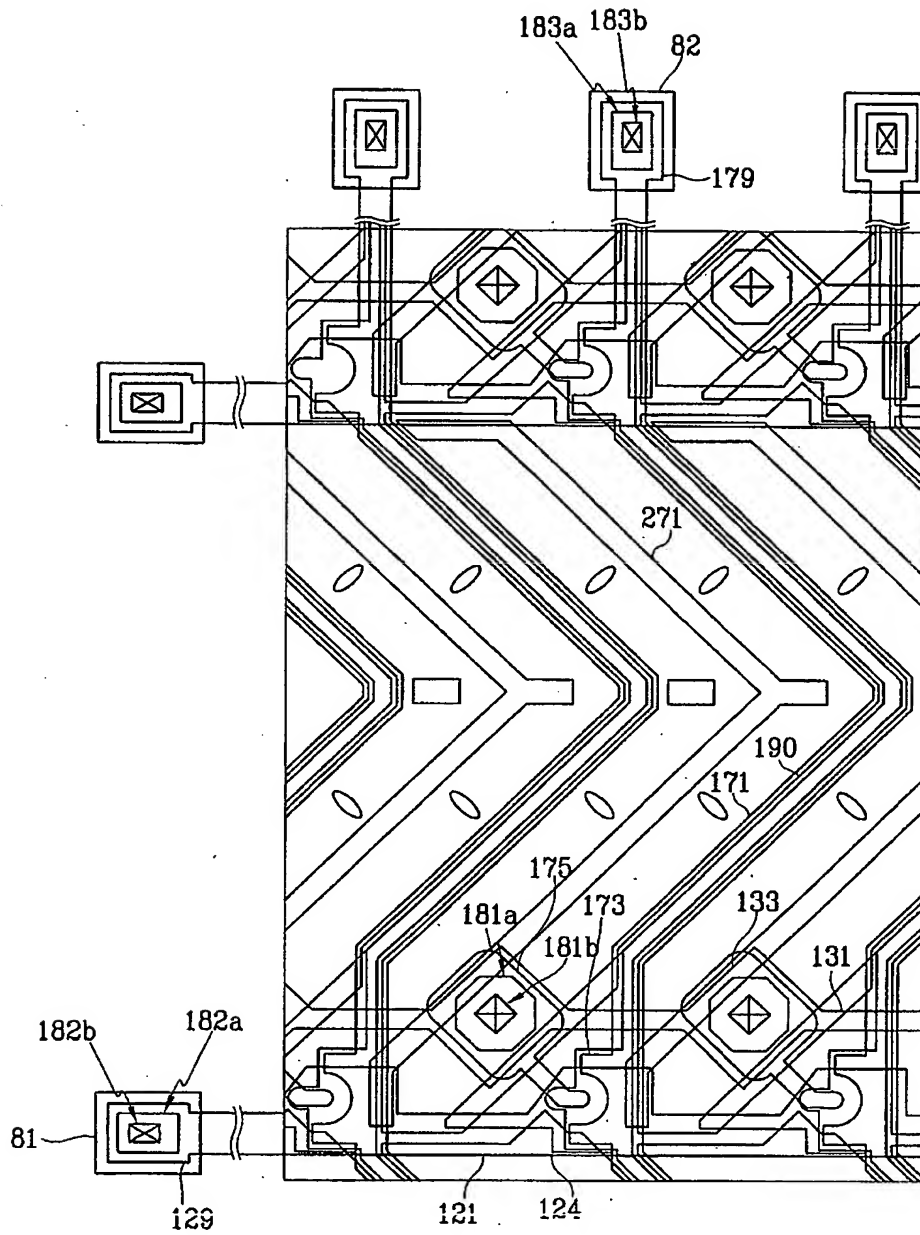


FIG.32

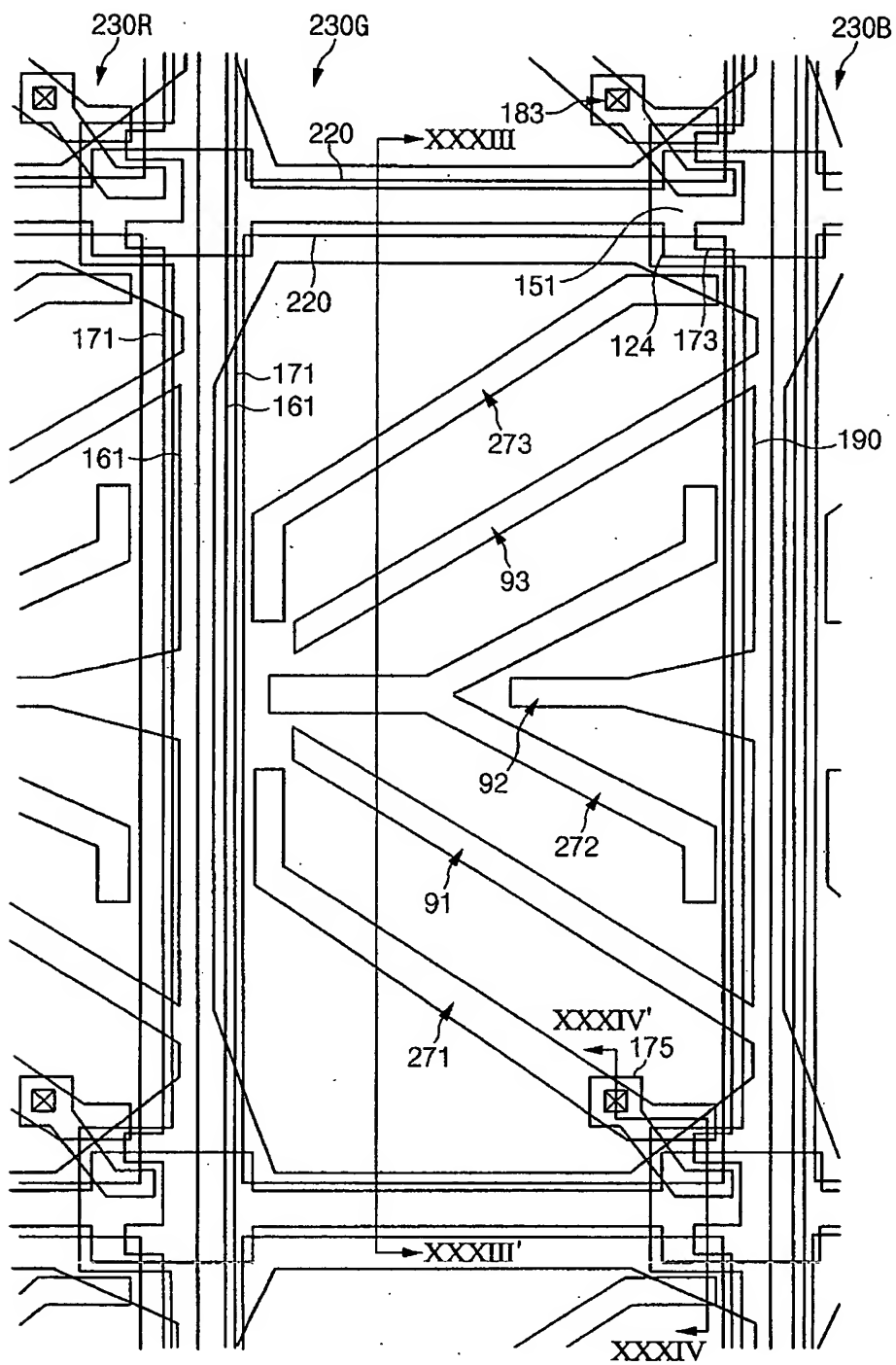




FIG.33

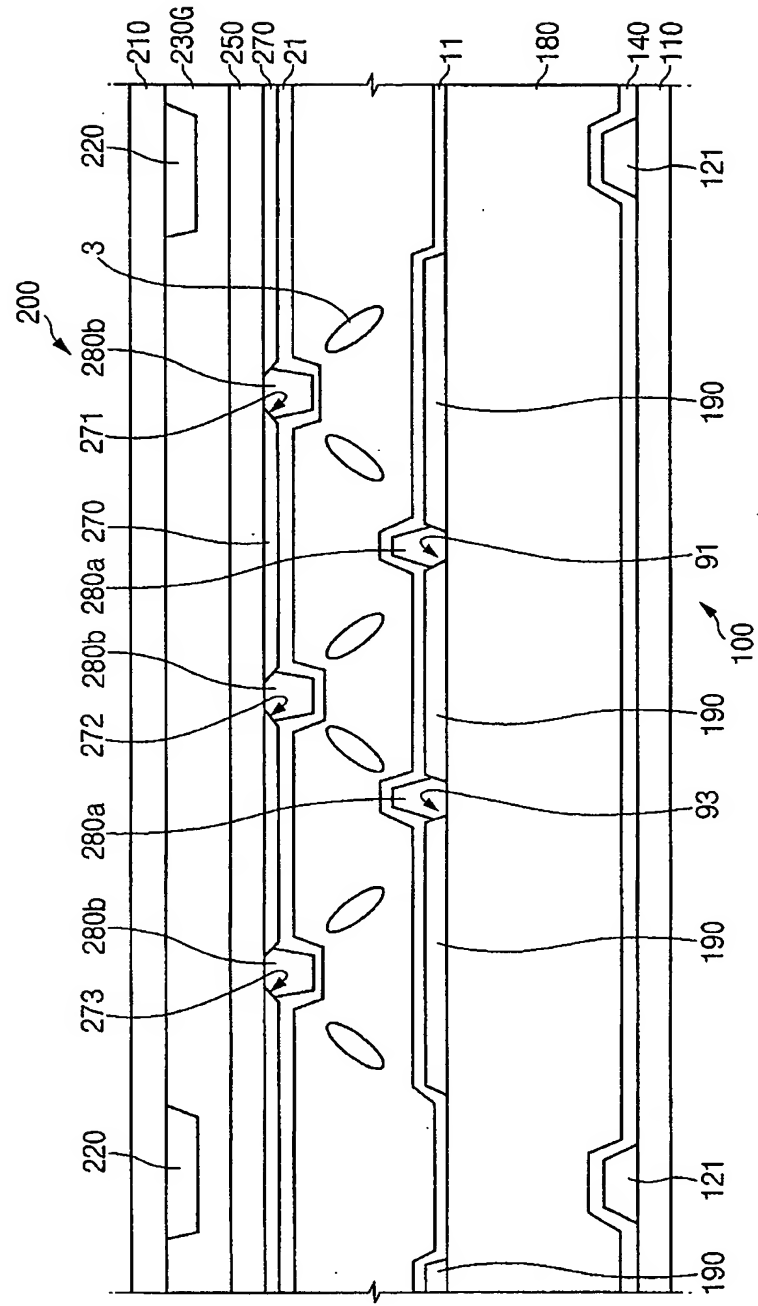


FIG.34

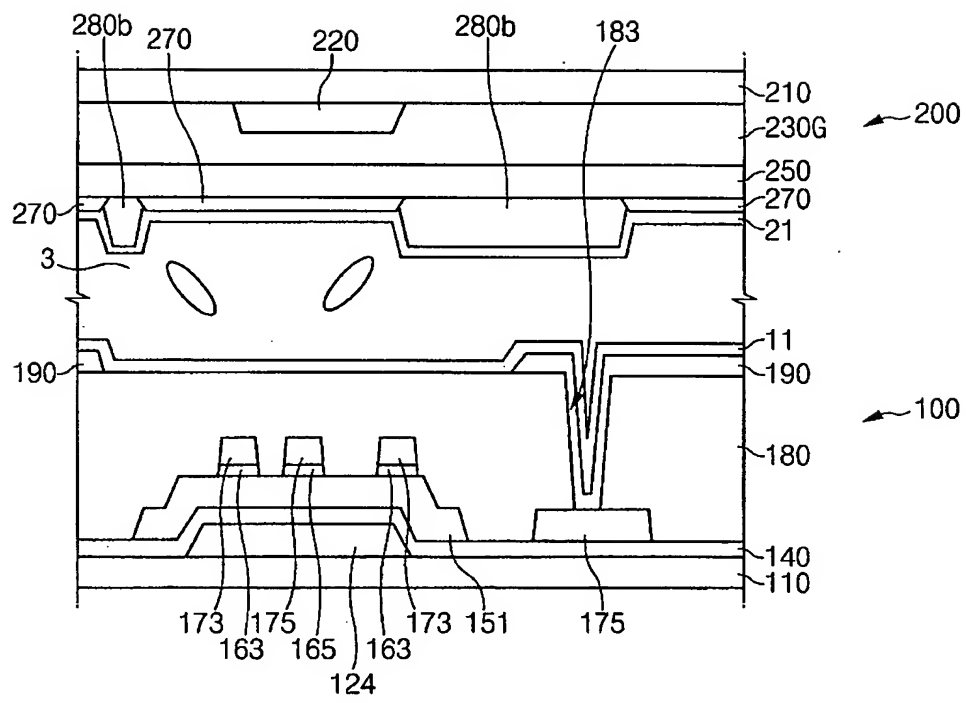


FIG.35

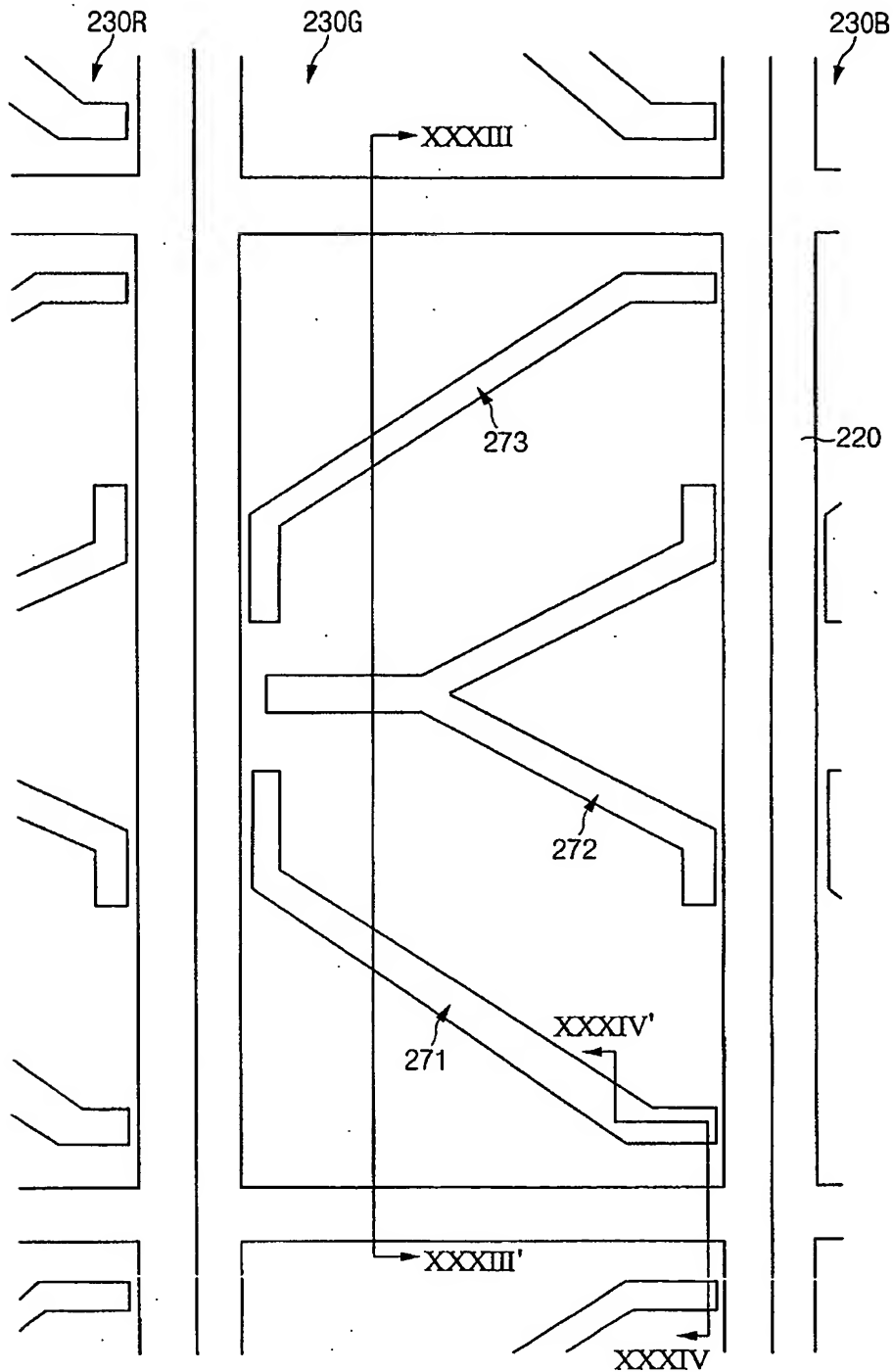


FIG.36

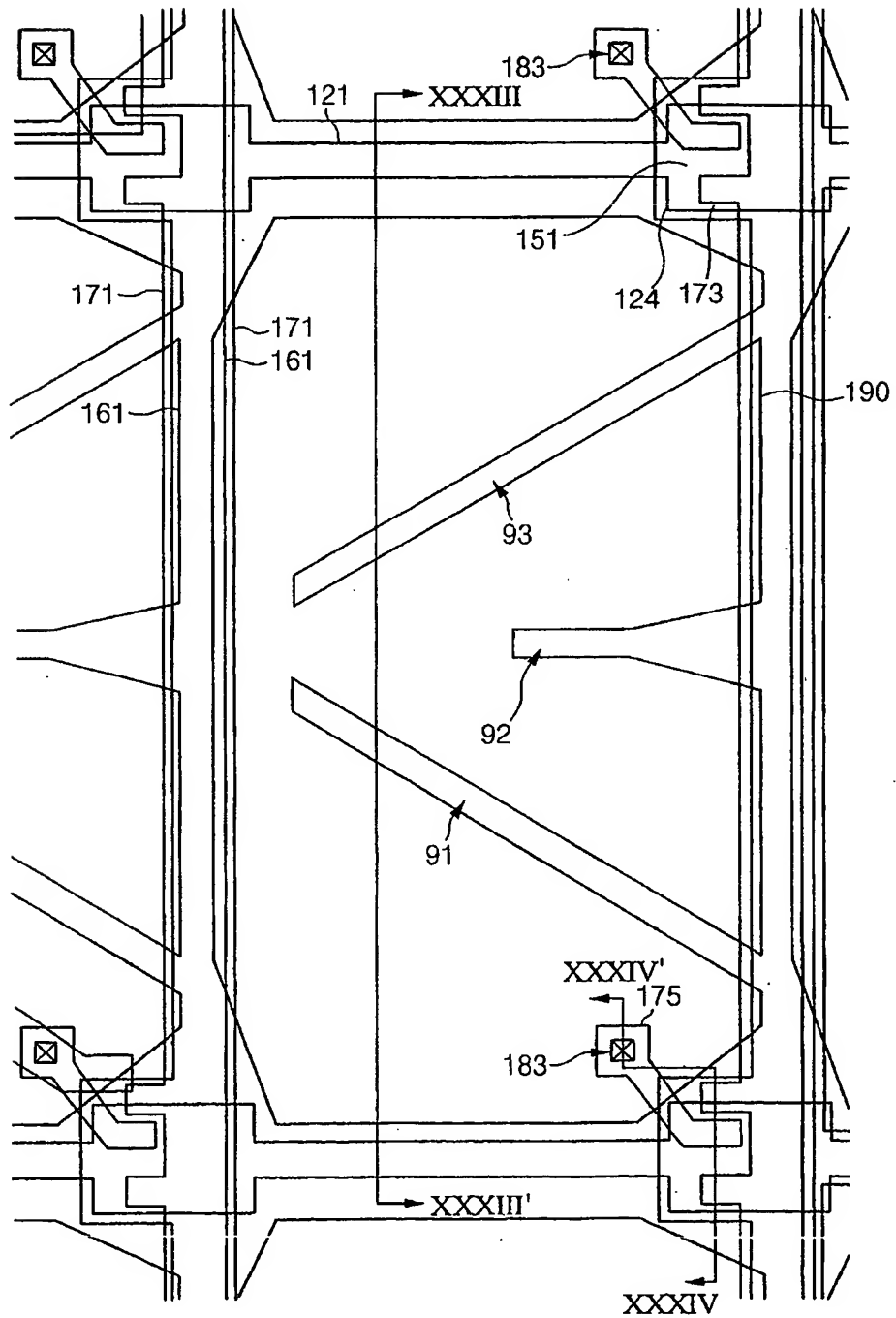


FIG.37

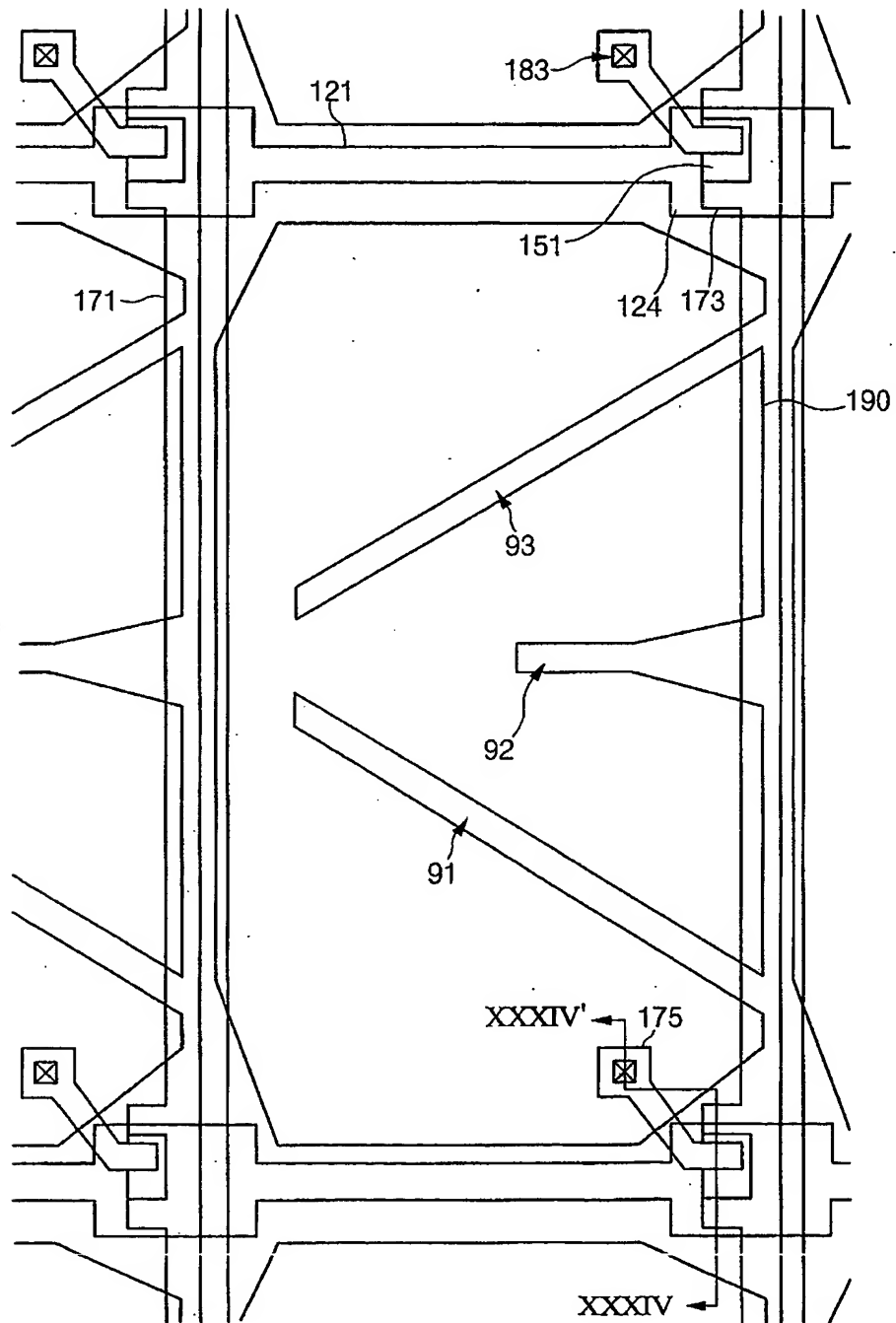


FIG.38

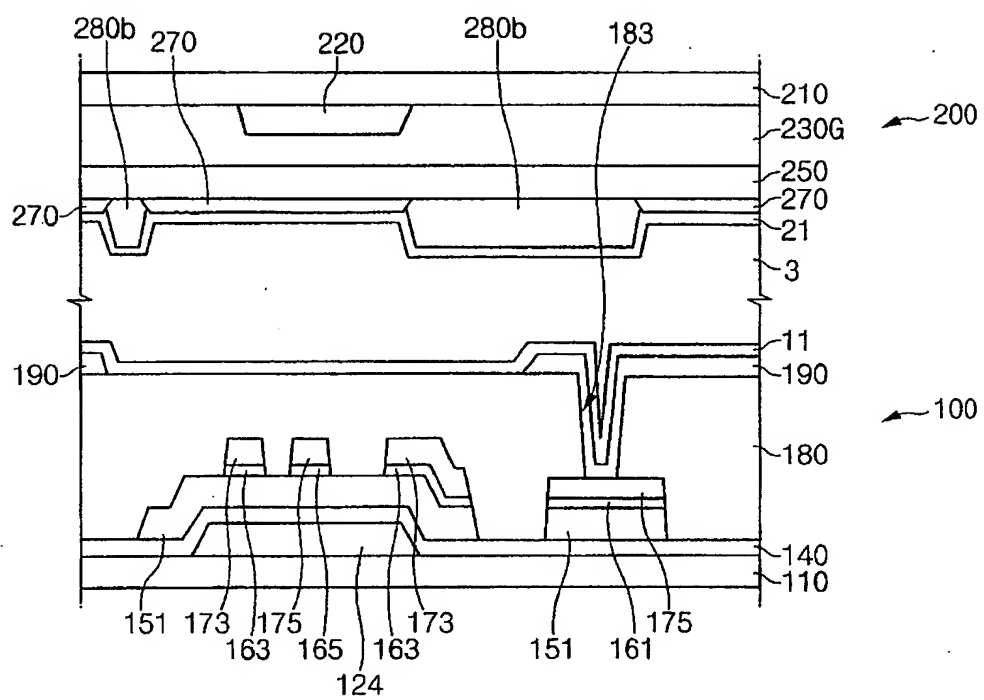


FIG. 39

